Comparison of Continuous and Discontinuous Current Source Drivers for High Frequency Applications*

Zhiliang Zhang （*Member IEEE*）

Aero-Power Sci-tech Center
College of Automation Engineering
Nanjing University of Aeronautics & Astronautics
Nanjing, Jiangsu, P.R.China
Email: zlzhang@nuaa.edu.cn

Jizhen Fu (*Student Member, IEEE*), Yan-Fei Liu (*Senior, Member IEEE*) and P.C. Sen (*Fellow IEEE*)
Department of Electrical and Computer Engineering
Queen's University, Kingston, Ontario, Canada
jizhen.fu@queensu.ca, yanfei.liu@queensu.ca and senp@post.queensu.ca

***Abstract* -- Comprehensive comparison of continuous and discontinuous Current Source Drivers (CSDs) are presented in terms of switching loss reduction, gate energy recovery, range of duty cycle and fast dynamic response. The advantages and disadvantages of the continuous and discontinuous CSDs are summarized. Overall, the discontinuous CSDs achieve better performance over the continuous CSDs. A 12V input, 1.3V/30A output and 1MHz buck converter was built to verify the difference between these two types of the CSDs.**

***Index Terms*—Current Source Driver (CSD), power MOSFET, Buck converter, Voltage Regulator (VR), Voltage Regulator Module (VRM), Resonant Gate Driver (RGD)**

I. INTRODUCTION

MHz switching frequency Voltage Regulators (VRs) for microprocessors are available in the industrial now, and show much better performance over the traditional VRs regarding the power density and dynamic response. However, MHz switching frequency results in high switching loss and gate drive loss, especially for synchronous rectifier (SR) MOSFETs with high total gate charge. Recently, Current Source Drivers (CSDs) becomes promising in MHz VRs to overcome the above problems. Similar to resonant gate drivers (soft drivers) [1]-[4], the CSDs can recover the gate drive energy and reduce gate drive loss. Furthermore, they are able to achieve significant switching loss reduction for the control MOSFETs in MHz VRs.

The dual channel low side CSD with one Current Source (CS) inductor was proposed for the interleaving boost converters in [5]. A dual channel high side and low side CSD using bootstrap technique was proposed to achieve the switching loss reduction and SR gate energy recovery in a buck converter in [6] and its improved version was presented in [7]. Based on an accurate analytical loss model, a general optimal method was proposed in [8] to find the trade off point of the switching losses and gate drive losses.

In order to reduce the CS inductor value, the CSD with discontinuous current was proposed in [9]-[10]. The key to this type of CSDs is to control of the driver switches to generate discontinuous inductor current waveforms enabling the peak portion of the current to be used to charge/discharge the power MOSFET as a nearly constant current source. A CSD with further reduced inductor value was also presented in [11]. In the above mentioned CSDs, the inductance value is typically 20nH at 1MHz switching frequency.

Considering the current waveforms of the CS inductors, the CSDs have two basic types: the continuous and the discontinuous. Presently, most of the work done with the CSDs is at the circuit level and based on design procedure for the specific CSD circuits. Moreover, no comprehensive comparison between the continuous and discontinuous CSDs has been reported in terms of the disadvantages and advantages. The idea of this paper is to provide some guidelines to choose which type of the CSDs should be used in some certain applications. Therefore, the continuous and discontinuous CSDs are evaluated thoroughly in terms of switching loss reduction, gate energy recovery, range of the duty cycle and fast response. The relationship between these two type CSDs are also revealed, which gives deep insights of the CSDs at high frequency.

II. CIRCUIT DESCRIPTIONS OF CONTINUOUS AND DISCONTINUOUS CSDS

In order to compare the properties of continuous and discontinuous CSDs, two basic CSDs are chosen here. Fig. 1 shows the continuous CSD circuit, which is the half-bridge topology and consists of two drive MOSFETs S_1 and S_2. V_c is the drive voltage, L_r is the current source inductor and C_b is the blocking capacitor.

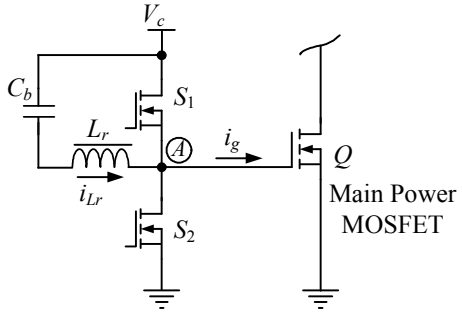


Fig. 1 Continuous CSD topology

This work is supported by NUAA Research Funding, No. NS2010087 and NJ2010016.

Fig. 2 gives the key waveforms. S_1 and S_2 are switched out of phase with complimentary control with ZVS. The inductor current is continuous and triangle. The peak portion of the inductor current is used to turn on and turn off the main power MOSFET Q during $[t_0, t_1]$ and $[t_2, t_3]$ as shown in Fig. 2 respectively.

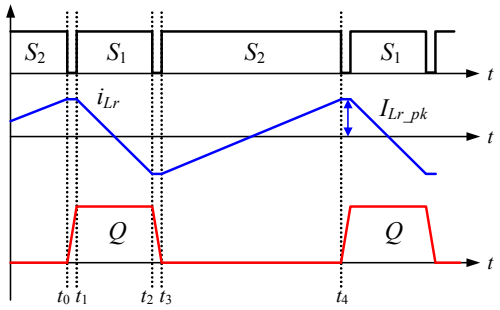


Fig. 2 Continuous CSD topology

Fig. 3 shows the discontinuous CSD circuit and Fig. 4 gives the key waveforms. In order to achieve discontinuous inductor current, S_3 and S_4 are inserted in series with the L_r and form a bidirectional switch, so that the current in the inductor can be controlled as desired. The key to this CSD is to control of the driver switches to generate discontinuous inductor current waveforms enabling the peak portion of the inductor current to be used to charge and discharge the power MOSFET gate capacitance as a nearly constant current source.

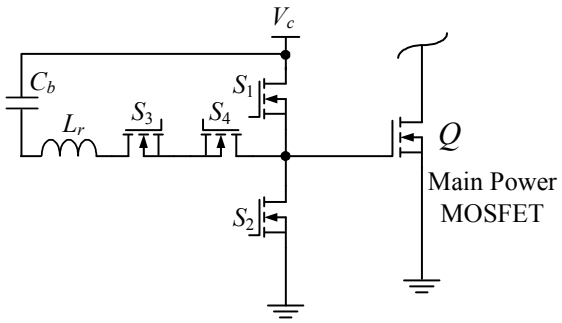


Fig. 3 Discontinuous CSD topology

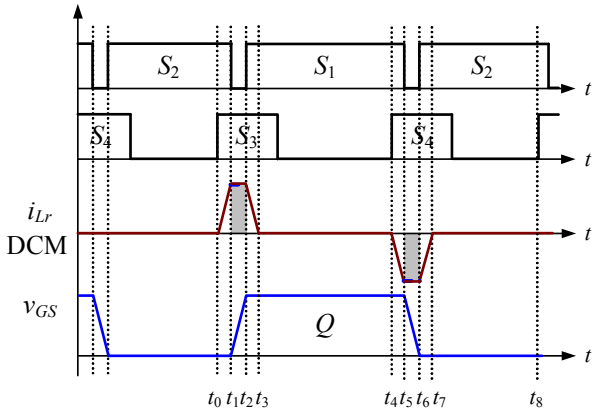


Fig. 4 Discontinuous key waveforms

Both of the two CSDs have two drive switches (S_1&S_2) to ensure low impedance path through the gate terminal to the drive voltage or the ground, which provides good noise immunity of the power MOSFET against *Cdv/dt* problem.

III. Comparison of Continuous and Discontinuous CSDs

A. Gate Energy Recovery

Both the continuous CSDs and discontinuous CSDs use the inductor as a current source. The energy stored in the inductance can be recovered to the driver supply voltage rail. The efficiency of gate energy recovery depends on the loss of the CSD circuit.

The drive loss includes: 1) the resistive loss caused by the impedance of the driver switches, P_{cond}, 2) the loss of the current source inductor L_r, P_{ind}; 3) the resistive loss caused by the internal gate mesh resistance of the power MOSFETs, P_{RG}; 4) gate drive loss of drive switches, P_{gate}.

Therefore, the total loss CSD is

$$P_{Drive} = P_{cond} + P_{ind} + P_{RG} + P_{gate} \quad (1)$$

Fig. 5 shows the drive loss comparison between the continuous and discontinuous at the switching frequency of 1 MHz. The components used are as follows: drive switches S_1-S_4: FDN335N; CS inductors: L_r=22nH (1812SMS) for the discontinuous, and L_r=1μH (DO1608C) for the continuous.

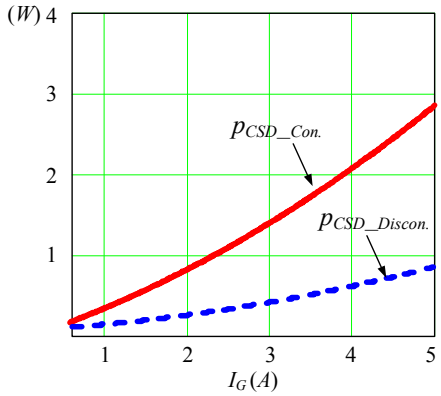


Fig. 5 Drive loss comparison between the continuous CSD and discontinuous CSD at 1MHz with different gate currents

It is observed that for the same gate drive current I_G, the discontinuous CSD has much lower drive loss than the continuous one, since the continuous current is a triangle waveform with larger RMS value and thus higher conduction loss.

B. Switching Loss Reduction

Both of the continuous and discontinuous CSDs can achieve fast switching speed and reduce the switching losses significantly since they can use the inductor current as constant current source.

For the continuous CSD, the peak value of the CS inductor current is the drive current, which is

$$I_G = I_{Lr\_pk} = \frac{V_c \cdot D \cdot (1-D)}{2 \cdot L_r \cdot f_s} \quad (2)$$

where V_c is the drive voltage, D is the duty cycle and L_r is CS inductor [7].

Normally, for the continuous CSDs, the current inductor value is relatively high, which is typically around 1μH at the switching frequency of 1MHz. Furthermore, the inductor value depends on the switching frequency, which makes the variable switching frequency control difficult. For example, when the switching frequency reduces from 1MHz to 500kHz, the peak value of the circulating current will double, which increase the drive circuit conduction losses of the drive switches and inductor by four times.

For the discontinuous CSD, referring to Fig. 4, the pre-charge current to turn on the power MOSFT is

$$I_{G\_on} = \frac{V_D}{2L_r} t_{10} \quad (3)$$

where V_D is the drive voltage and t_{10} is the pre-charge interval [11].

Similarly, the pre-charge current to turn off the power MOSFET is

$$I_{G\_off} = \frac{V_{Cs}}{L_r} \cdot t_{54} = \frac{V_D}{2L_r} \cdot t_{54} \quad (4)$$

where V_{Cs} is the DC voltage across the capacitor.

In comparison, the discontinuous CSD has much lower inductor value, which is around 20nH at 1MHz switching frequency typically. This significant inductance reduction leads to the size shrink and board area reduction. More importantly, the inductance is independent of the switching frequency so that variable frequency control can be used with this type of CSDs.

Furthermore, the discontinuous CSD has discontinuous inductor current and thus low conduction losses, so higher drive current can be used to reduce switching losses compared to the continuous one.

For a given application, in order to achieve fast switching speed, the gate drive current should be chosen properly. The design tradeoff is between switching speed, which translates into reduced switching loss, and gate drive loss.

The basic idea is to find the optimal solution on the basis of the object function that adds the switching loss and the CSD circuit loss together. The object function is a U-shape curve as function of the drive current I_G, and the optimization solution is simply located at the lowest point of the curve.

Based on the same idea, Fig. 6 and Fig. 7 illustrate the optimal curve for the discontinuous and continuous CSDs respectively, which includes the switching loss $p\_{switching\ loss}$, the CSD circuit loss $p\_{CSD\ circuit}$ and the objective function $F(I_G)$ as function of the gate drive current I_G. The specifications of the buck converter are: V_{in}=12V; V_o=1.3V; I_o=30A; V_c=5V; f_s=1MHz; control MOSFET Q_1: Si7386DP; Q_2: IRF6691 and L_f=330nH.

It is observed that $F(I_G)$ is a U-shaped curve, and therefore, the optimization solution can be found at the lowest point of the curve. For the discontinuous CSD, the optimal drive current I_G is chosen as 2.3A, while the optimal drive current is 1.2A for the continuous one. This is because the continuous CSD has higher drive circulating loss over the discontinuous one as shown in Fig. 5, which limits the optimal drive current value.

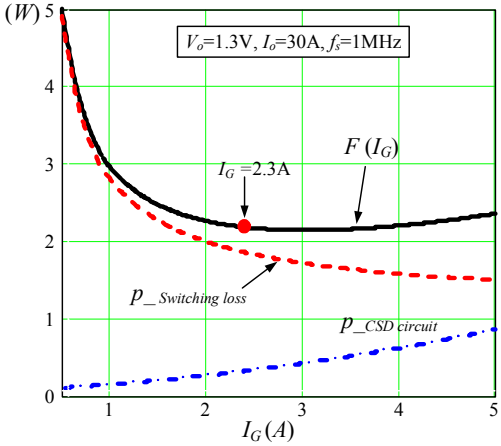


Fig. 6 Optimal function $F(I_G)$ as function of current I_G: discontinuous

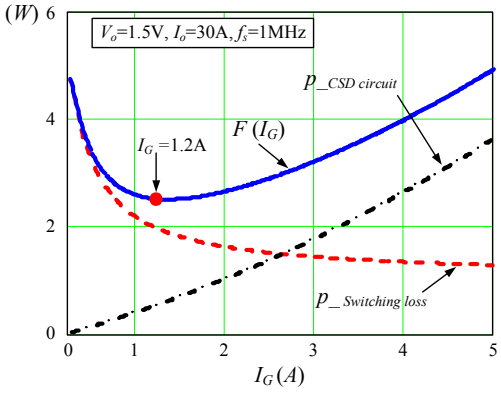


Fig. 7 Optimal function $F(I_G)$ as function of current I_G: continuous

C. *Range of Duty Cycle and Switching Frequency*

In a high frequency buck converter, the duty cycle is required to change fast during a transient event. At the same time, in order to improve the efficiency in a wide load range, the switching frequency of a buck converter may need to vary according to the load condition.

In order to ramp up the inductor current, the discontinuous CSDs need to have some pre-charge time. The pre-charge time and switching transition time lead to the minimum and maximum duty cycle range.

Fig. 8 illustrates the waveforms of the minimum duty cycle. As seen from Fig. 4, when the duty cycle reduces, the time from t_4 to t_3 (t_{43}) reduces accordingly, until Fig. 4 changes into Fig. 8.

From Fig. 8 and (3), the energy recovery time t_{32} is

$$t_{32} = \frac{I_{G\_on} \cdot L_r}{V_{Cs}} = \frac{I_{G\_on} \cdot L_r}{V_D / 2} = \frac{2I_{G\_on} \cdot L_r}{V_D} \tag{5}$$

From Fig. 8 and (5), the minimum t_{min} is

$$t_{\min} = t_{32} + t_{54} = \frac{2I_{G\_on} \cdot L_r}{V_D} + t_{54} \tag{6}$$

where t_{54} is the pre-charge time for turn off current. Therefore, from (6), the minimum duty cycle D_{min} is

$$\begin{aligned} D_{\min} &= \frac{t_{\min}}{T_s} = \frac{2I_{G\_on} \cdot L_r}{V_D T_s} + \frac{t_{54}}{T_s} \\ &= (\frac{2I_{G\_on} \cdot L_r}{V_D} + t_{54}) f_s \end{aligned} \tag{7}$$

where f_s is the switching frequency.

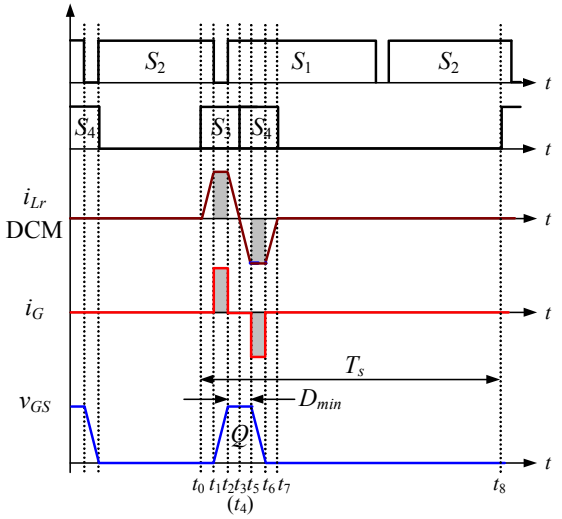


Fig. 8 Key waveforms with minimum duty cycle

As an example, Fig. 9 shows the minimum duty cycle as the function of the switching frequency, where I_{G_on}=2.3A, L_r=22nH, V_D=5V and t_{54}=15ns. It is observed that D_{min} increases when the switching frequency increases, and particularly, at f_s=1MHz, D_{min} is 0.035, which is small enough for most applications.

From (7), if we have the minimum duty cycle requirement as D_{min_req}, the switching frequency should meet

$$f_s \le \frac{D_{\min\_req}}{\frac{2I_{G\_on} \cdot L_r}{V_D} + t_{54}} \tag{8}$$

Fig. 10 illustrates the waveforms of the maximum duty cycle. As seen from Fig. 4, when the duty cycle increases, the time from t_8 to t_7 (t_{87}) reduces accordingly, until Fig. 4 changes into Fig. 10.

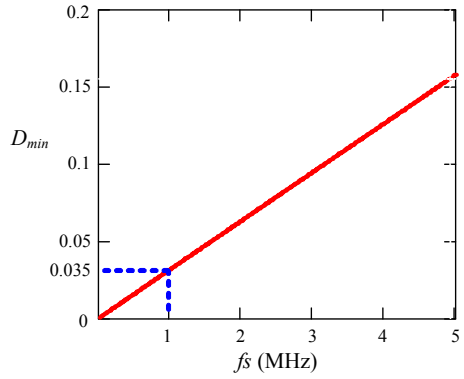


Fig. 9 The minimum duty cycle vs. the switching frequency

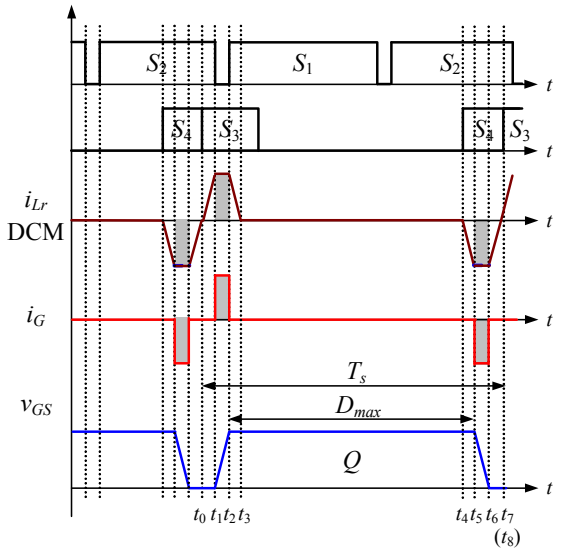


Fig. 10 Key waveforms with maximum duty cycle

From Fig. 10, the turn on time t_{21} is

$$t_{21} = \frac{C_{gs} V_D}{I_{G\_on}} \tag{9}$$

From (4), the turn off time t_{65} is

$$t_{65} = \frac{C_{gs} V_D}{I_{G\_off}} \tag{10}$$

From Fig. 8, the energy recovery time t_{76} is

$$t_{76} = \frac{2I_{G\_off} \cdot L_r}{V_D} \tag{11}$$

From (9), (10) and (11), the maximum time t_{max} is

$$\begin{aligned} t_{\max} &= T_s - t_{10} - t_{21} - t_{65} - t_{76} \\ &= T_s - t_{10} - \frac{C_{gs} V_D}{I_{G\_on}} - \frac{C_{gs} V_D}{I_{G\_off}} - \frac{2I_{G\_off} \cdot L_r}{V_D} \end{aligned} \tag{12}$$

Therefore, from (12), the maximum duty cycle D_{max} is

$$D_{\max} = \frac{t_{\max}}{T_s} =$$
$$1 - \frac{t_{10}}{T_s} - \frac{C_{gs}V_D}{I_{G\_on}T_s} - \frac{C_{gs}V_D}{I_{G\_off}T_s} - \frac{2I_{G\_off}\cdot L_r}{V_D T_s} \quad (13)$$
$$= 1 - (t_{10} + \frac{C_{gs}V_D}{I_{G\_on}} + \frac{C_{gs}V_D}{I_{G\_off}} + \frac{2I_{G\_off}\cdot L_r}{V_D}) f_s$$

As an example, Fig. 11 shows the maximum duty cycle as the function of the switching frequency, where for I_{G_on}=I_{G_off}=2.3A, C_{gs}=1.6nF, L_r=22nH, V_D=5V and t_{10}=15ns. It is observed that D_{max} decreases when the switching frequency increases, and particularly, at f_s=1MHz, D_{max} is 0.96, which is large enough for most application.

From (13), if we have the maximum duty cycle requirement as D_{max_req}, the switching frequency should meet

$$f_s \le \frac{1 - D_{\max\_req}}{t_{10} + \frac{C_{gs}V_D}{I_{G\_on}} + \frac{C_{gs}V_D}{I_{G\_off}} + \frac{2I_{G\_off}\cdot L_r}{V_D}} \quad (14)$$

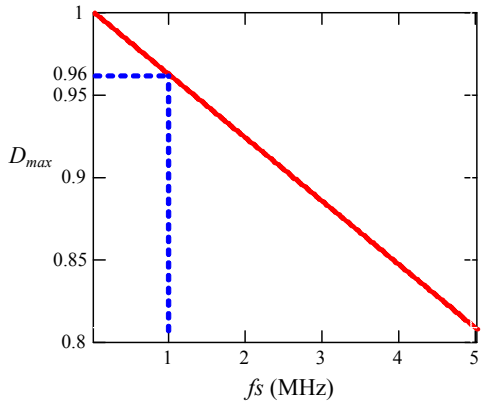


Fig. 11 The maximum duty cycle vs. the switching frequency

As a conclusion, the discontinuous CSD can operate correctly with the minimum duty cycle of 0.035 and maximum duty cycle of 0.96 with the 1MHz switching frequency.

For some extreme conditions, we can add extra logic circuits to achieve the duty cycle of zero or 100%. So it is suitable for different types of control and wide operating conditions.

D. *Fast Duty Cycle Change*

In many applications, the control commands require the step changes of the duty cycle, such as the linear-nolinear-control and charge balance control to improve the dynamic performance, especially for VRM applications [12]-[14].

In Fig. 1, using volt-second balance across the current source inductor, the DC voltage, v_{cb}, across the blocking capacitor, C_b, is

$$v_{Cb1} = (1 - D)\cdot V_c \quad (15)$$

where D is the duty cycle.

From (15), the drawback of the continuous CSDs in Fig. 1 is that the voltage across the blocking capacitor C_b changes with duty cycle. This limits the speed of the response when the duty cycle has step changes.

In Fig. 3, assuming t_{10}=t_{32}, the DC voltage across the series capacitor is self regulated as

$$V_{Cs} = \frac{V_D}{2} \quad (16)$$

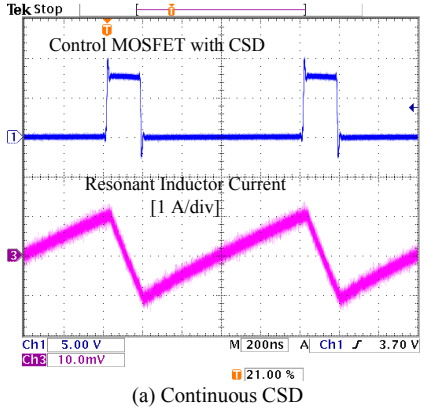
It is noted that the voltage across the capacitor no longer depends on the duty cycle. Therefore, the discontinuous CSD have better performance when the step changes of the duty cycle happen.

IV. Experimental Results and Discussion

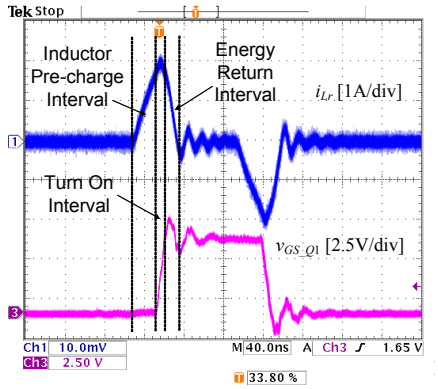
A 12V input, 1.3V/30A output and 1MHz buck converter was built to verify the comparison of the continuous and the discontinuous CSDs. The CSDs are used for the control MOSFET and conventional voltage source driver is used for the SR MOSFET. The gate driver voltage V_c=6 V. The PCB uses six-layer 2 oz copper. The components used are: Q_1: Si7860DP; Q_2: irf6691; output filter inductance: L_f=300nH. For the continuous CSD, L_r=1μH; for the discontinuous CSD, L_r=22nH.

Fig. 12(a) shows the CS inductor current i_{Lr} and the gate drive signals v_{GS_Q1} (control MOSFET) with the continuous CSD. The inductor current is triangle waveform and its peak current value is 1.2 A, which is the optimized value for the switching loss reduction.

In comparison, Fig. 12(b) illustrates the waveforms of i_{Lr} and v_{GS_Q1} for discontinuous CSD. The inductor current is discontinuous as expected. During the pre-charge time, the inductor current ramps up. After the designed the pre-charge time, the inductor current continues to ramp up at a decreasing rate while at the same time charge the gate of the control MOSFET during the turn on interval. During this interval the average drive current is approximately 2.0A. It is noted that due to discontinuous current, higher drive current can be used in the discontinuous CSD to achieve faster drive speed.



(a) Continuous CSD



(b) Discontinuous CSD

Fig. 12 Gate signals v_{gs_Q1} and CS inductor current i_{Lr}

Fig. 13 and Fig. 14 illustrate the duty cycle changes from D=0.1 to D=0.9, for the continuous and discontinuous CSDs respectively. It is observed that the continuous CSD gate voltage needs time to change due to the blocking capacitor, while the discontinuous one is able to response simultaneously. This is of great benefit for the VR application with fast dynamic response requirement.

Fig. 15 shows the efficiency comparison. They both achieve higher efficiency over the conventional voltage driver. The discontinuous CSD achieves higher efficiency over the continuous CSD due to higher gate drive current.

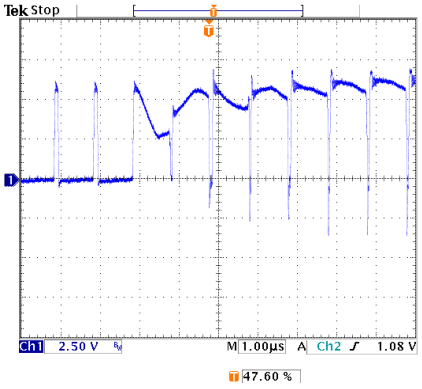


Fig. 13 Gate signals v_{gs_Q1} from D=0.1 to D=0.9: continuous

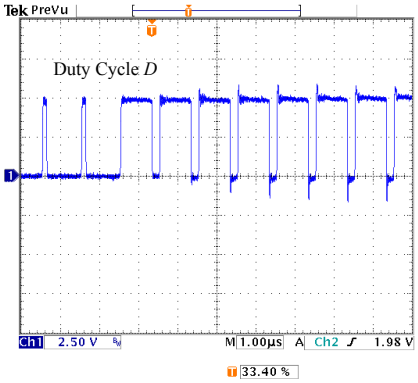


Fig. 14 Gate signals v_{GS_Q1} from D=0.1 to D=0.8: discontinuous

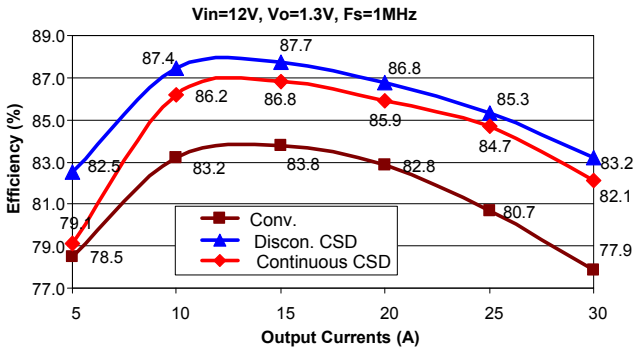


Fig. 15 Efficiency at different output voltages

V. Conclusion

In this paper, comprehensive comparison of continuous and discontinuous CSDs are presented in terms of switching loss reduction, gate energy recovery, range of duty cycle and switching frequency. Compared to the continuous CSDs, the discontinuous CSDs can achieve high gate drive current and low drive circuit losses. They are more suitable for applications with wide range of duty cycle and switching frequency as well as quick step duty cycle change.

Nevertheless, the discontinuous CSDs need more drive switches and complex control. Owing to the integrated circuit technology, this drawback can be solved when the CSDs are integrated as a drive chip. The experimental results verified the difference of the two types of the CSD circuits.

References

[1] D. Maksimovic, "A MOS gate drive with resonant transitions," in *Proc. IEEE PESC*, 1991, pp. 527-532.

[2] G. Spiazzi; P. Mattavelli and L. Rossetto, "Effects of parasitic components in high-frequency resonant drivers for synchronous rectification MOSFETs," *IEEE Trans. on Power Electronics*, Vol. 23, No. 4, pp. 2082–2092. Jul. 2008.

[3] J. R. Warren, K. A. Rosowski and D. J. Perreault, "Transistor selection and design of a VHF DC-DC power converter," *IEEE Trans. on Power Electronics*, Vol. 23, No. 1, pp.27 – 37, Jan. 2008.

[4] Y. Ren, M. Xu, Y. Meng and F. C. Lee, "12V VR efficiency improvement based on two-stage approach and a novel gate driver," in *Proc. IEEE PESC*, 2005, pp. 2635-2641.

[5] Z. Yang, S. Ye, and Y. F. Liu, "New dual channel resonant gate drive circuit for low gate drive loss and low switching loss", *IEEE Trans. on Power Electronics*, Vol. 23, No. 3, pp. 1574-1583, May 2008.

[6] Z. Yang, S. Ye and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," *IEEE Trans. Power Electron*., Vol. 22, No. 4, pp.1311-1320, July 2007.

[7] Z. Zhang, W. Eberle, P. Lin, Y. F. Liu and P. C. Sen, "A 1-MHz high efficiency 12V buck voltage regulator with a new current-source gate driver," *IEEE Trans. Power Electron*., Vol. 23, No. 6, Nov. 2008, pp. 2817-2827.

[8] W. Eberle, Z. Zhang, Y. F. Liu and P. C. Sen, "A practical switching loss model for buck voltage regulators," *IEEE Trans. Power Electron*., Vol. 24, No. 3, Mar. 2009, pp. 700-713.

[9] W. Eberle, Z. Zhang, Y. F. Liu and P. C. Sen, 'A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz," *IEEE Trans. Power Electron*., Vol. 23, No. 2, Mar. 2008, pp. 678 -691.

[10] S. Pan and P. K. Jain, "A new pulse resonant MOSFET gate driver with efficient energy recovery," in *Proc. IEEE PESC*, 2006, pp. 1-5.

[11] Z. Zhang, J. Fu, Y. F. Liu and P. C. Sen, "A new discontinuous

current-source driver for high frequency power MOSFETs," in *Proc. IEEE ECCE* 2009, pp. 1655-1662.
[12] E. Meyer, Z. Zhang, and Y.-F. Liu, "An optimal control method for buck converters using a practical capacitor charge balance technique," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1802–1812, Jul. 2008.
[13] A. Soto, P. Alou, and J. A. Cobos, "Nonlinear digital control breaks bandwidth limitations," in *Proc. IEEE APEC*, 2006, pp. 724–730.
[14] Z. Zhao and A. Prodic, "Continuous-time digital controller for high frequency DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, No. 2, pp. 564–373, Mar. 2008.